A New Technique of Electro-thermal Modeling and Reliability Circuit Analysis of Power MOSFETs with Mathematica

Tamiyo Nakabayashi[†], Keiji Nakabayashi[‡], and Fujio Kako[†]
[†]Nara Women's University
Kitauoyahigashi-machi, Nara, Japan
{nakaba, kako}@ ics.nara-wu.ac.jp
[‡]WDB Corporation
Azuchi-machi, Chuo-ku, Osaka, Japan
nakaba62@hotmail.com

Abstract: - We propose a new equation-based modeling technique for electro-thermal and reliability circuit analysis of power MOSFET circuits with Mathematica. We express the electrical characteristics and self-heating effect of a power MOSFET as a system of ordinary differential equations, and use a numerical solver of Mathemtica to obtain a solution of the system. We explain the technique using an Unclamped Inductive Switching (UIS) test circuit. Our experimental results demonstrate the adequacy of our technique for the electro-thermal modeling and circuit analysis. They also reveal that the numerical solver of Mathematica is capable of circuit analysis such as that of SPICE (a circuit simulator).

Key-Words: - electro-thermal coupling, equation-based modeling, reliability circuit analysis, Power MOSFET circuits, Mathematica, ordinary differential equation, SPICE.

1 Introduction

Mathematica is worldwide software of symbolic analysis (computer algebra) and numerical analysis, and it is used in science, engineering, mathematics, and other areas [11].

In the area of electronic/electrical circuits design, Mathematica is applied to symbolic circuit analysis for analog circuits [1], [2], [6], [7]. The target of these previous researches is small signal analysis and transfer function modeling (frequency domain) for linear analog circuits, the circuits of which are composed of a number of resistors, capacitors, inductors, macro cells (models) of operational amplifiers, and so on.

Furthermore, in the Wolfram Demonstrations Project (circuit design) some examples of equation-based modeling for very simple electronic circuits are exhibited [4]. In the research of [12], computer algebra approach with Mathematica is applied to the symbolic analysis for a power supply stabilization loop circuit. This work obtains a set of optimized design parameters by solving an equivalent system of non-linear algebra equations that express the circuit structure and its frequency domain characteristics.

Recently, we proposed a technique for simple electro-thermal equivalent circuit level modeling and reliability circuit simulation of power MOSFETs (MOSFETs) with SystemC-AMS/NGSPICE [13], [18]. As a case study, we focused on an Unclamped Inductive Switching (UIS) test circuit that is used for an avalanche breakdown test of MOSFETs. The avalanche breakdown (breakdown) is affected by device junction temperature rise that is due to self-heating of MOSFETs. In the reliability circuit simulation, it is essential that coupling of the electrical behaviour and thermal behaviour (electrical-thermal coupling) is considered [5], [9]-[10], [15], [16], [19].

The goal of our research in this paper is to present a new technique equation-based electro-thermal coupling modeling and transient (time domain) analysis of MOSFETs with Mathematica. First we derive a system of ordinary differential equations, which express the current-voltage characteristics (I-V characteristics) and the electrical-thermal coupling of MOSFETs. Next we implement the system into Mathematica, and solve it. Finally we demonstrate our technique by several test results with the UIS test circuit.

In the next section, we explain an Unclamped Inductive Switching (UIS) test circuit. Section III describes our equation-based electro-thermal power MOSFET model and circuit analysis technique with Mathematica. Section IV describes

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our experiments and compares the results. We conclude the paper in Section V.

NOMENCLATURE

Power MOSFET

t	Simulation time domain [sec]
T_{nom}	Room temperature [K]
β	MOSFET channel conductance [A/V^2]
β_0	Value of β at T_{nom} [A/V^2]
V_{th}	Threshold voltage [V]
V_{th0}	Value of V_{th} at T_{nom} [V]
V_{gs}	Gate-source voltage [V]
V_{ds}	Drain-source voltage [V]
C_{gs}	Gate-source capacitance [F]
C_{ds}	Drain-source capacitance [F]
C_{gd}	Gate-drain capacitance [F]
$R_{on(mos)}$	Drain-source on resistance [Ohm]
$R_{off(mos)}$	Drain-source off resistance [Ohm]
R_{ds}	Drain-source resistance [Ohm]
G_{ds}	Drain-source conductance [1/Ohm] ($R_{ds} = 1/G_{ds}$)
I_{ds}	Drain-source current [A]
TCV_{th}	Temperature coefficient of V_{th} [1/K]
$TC\beta$	Temperature coefficient of β [-]
BV_{dss}	Avalanche breakdown voltage at T_{nom} [V]
$BV_{dss(eff)}$	Effective avalanche breakdown voltage [V]
R_{mos_body}	MOSFET body resistance [Ohm]
V_{dd}	Power supply voltage [V]
V_{gg}	Pulse voltage source [V]
L_{drain}	Drain load inductance [H]
R_{drain}	Drain load resistance [Ohm]
R_{gate}	Gate resistance [Ohm]
P_{mos}	MOSFET power dissipation [W]
T_j	Device junction temperature [K] (Nodal voltage at thermal node)

Diode

V_{on}	Diode on voltage [V]
V_{pn}	Diode pn junction voltage [V]
$R_{on(diode)}$	Diode on resistance [Ohm]
$R_{off(diode)}$	Diode off resistance [Ohm]
$R_{on(body)}$	Body diode on resistance [Ohm]
$R_{off(body)}$	Body diode off resistance [Ohm]
$R_{on(bkdn)}$	Breakdown diode on resistance [Ohm]
$R_{off(bkdn)}$	Breakdown diode off resistance [Ohm]
V_{br}	Breakdown voltage [V] (V_{br}= $BV_{dss(eff)}$)

Thermal Circuit

T_{thi}	Device junction-case temperature rise [K]
C_{thi}	Device junction-case thermal capacitance [J/K]
R_{thi}	Device junction-case thermal resistance [K/W] (The index i ranges as $i = 1, 2, \ldots, 6$)
T_{case}	Case temperature [K]
T_{amb}	Ambient temperature [K] (T_{amb}= T_{nom})
V_{amb}	Ambient temperature definition [K] ($V_{amb} = T_{amb}$)
T_{thp}	Case-ambient temperature rise [K] ($T_{thp} = T_{case} - T_{nom}$)
C_{thp}	Case-ambient thermal capacitance [J/K]
R_{thp}	Case-ambient thermal resistance [K/W]

2 Unclamped Inductive Switching Test Circuit

An UIS test circuit is used to evaluate tolerance for the avalanche breakdown (breakdown) that is the most important reliability assessment of power MOSFETs. Figure. 2.1 depicts the schematic of the UIS test circuit that is used in [5], [9]-[10], [13]. The UIS test circuit is a steep switching circuit that is composed of a MOSFET (switching device), and a parasitic inductor (load device). The counter electromagnetic force that is induced by the inductance causes a significant over voltage transient between drain and source of the MOSFET. If the resulting voltage transient is large enough, the MOSFET is forced into the drain-source avalanche breakdown. The high drain-source current causes its device junction temperature rise that is due to self-heating effect. The device junction temperature rise affects the avalanche breakdown voltage and electrical characteristics of the MOSFET [9]-[10], [13], [15].

It is very important that the device junction temperature rise that is due to self-heating effect is reflected to the MOSFET characteristics. In the UIS test circuit, particularly, the on/off switching drain-source resistance and avalanche breakdown of the MOSFET are important characteristics, which have temperature dependence. Therefore, the electro-thermal device model that incorporates with the self-heating effect and electrical characteristics is essential in the UIS test circuit simulation for tolerance evaluation of the avalanche breakdown [5], [9]-[10], [13].

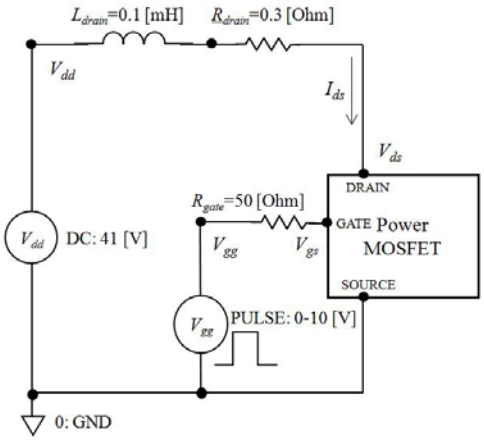


Fig. 2.1: Unclamped Inductive Switching test circuit [5], [9]-[10], [13].

3 Our Equation-Based Modeling

We apply our equation-based modeling to an UIS circuit. The circuit is composed of an electronic circuit and a thermal circuit, as depicted in Fig. 3.1. The electronic circuit include a power MOSFET and its simple electrical equivalent circuit model is depicted in Fig. 3.2 [13]. And the thermal circuit include a thermal equivalent circuit model from device junction (T_j) to package case (T_{case}), which is depicted in Fig. 3.2.

The power dissipation (G_{mos_pwr}) of the MOSFET flows into the thermal equivalent circuit model as a current source, and the device junction temperature (T_j) is calculated as a nodal voltage. The device junction temperature is fed back to the electrical equivalent circuit model as thermal nodal voltage of the MOSFET. Then, the values of very important parameters with (device) temperature dependence such as threshold voltage, channel conductance (G_{ds}), effective avalanche breakdown voltage ($BV_{dss(eff)}$), and so on are updated.

Based on the updated values, next computation process goes. A series of computation processes is repeated at each time step in electro-thermal circuit analysis. The thermal equivalent circuit model is a linear network that composed of thermal resistances (R_{thi}) and thermal capacitances (C_{thi}), which expresses thermal conduction from device junction (T_j) to package case (T_{case}). Note that i = 1, 2, …, 6. And the thermal conduction from package case (T_{case}) to ambient (T_{amb}) is expressed as a linear circuit that compose of a thermal resistance (R_{thp}) and a thermal capacitance (C_{thp}).

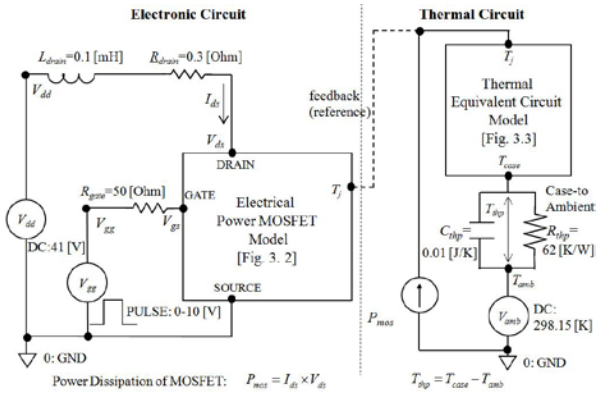


Fig. 3.1: Schematic for the electro-thermal simulations of an UIS test circuit.

We model the UIS test circuit depicted in Fig. 3.1 as a system of ordinary differential equations. Note that source node (SOURCE) is connected to ground (GND). First we define a drain-source function that expresses the drain-source conductance of the MOSFET (G_{ds}), and express it as Eq. (3-1). The function is equivalent to the current-voltage (I-V) characteristics of the MOSFET, and is used at our simple power MOSFET electrical model [13] depicted in Fig. 3.2. It has temperature dependence such as threshold voltage and channel conductance, which is described by Eqs. (3-2) and (3-3).

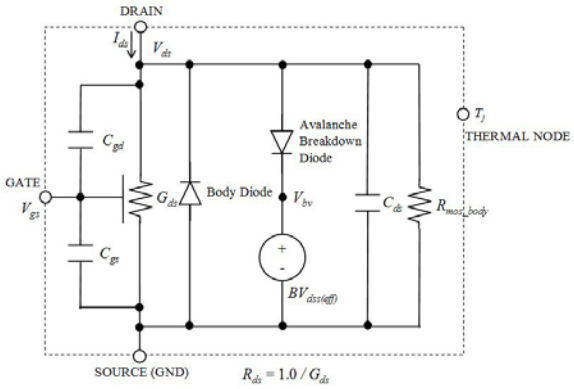


Fig. 3.2: our simple electrical power MOSFET model [13].

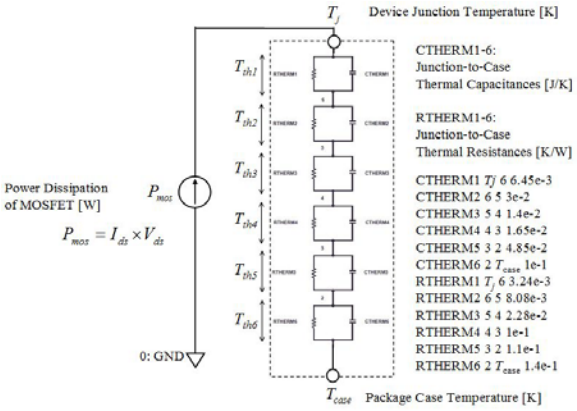


Fig. 3.3: thermal equivalent circuit model of electro-thermal power MOSFET model [5], [9]-[10].

$$G_{ds}(V_{gs}, V_{th}, \beta, R_{off\,(mos)}) := Max(Tanh(V_{gs} - V_{th}), 0.0) \times \beta(V_{gs} - V_{th}) + \left(\frac{1.0}{R_{off\,(mos)}}\right) \quad (3\text{-}1)$$

where

$$V_{th} = V_{th0} \times (1.0 + TCV_{th} \times (T_j - T_{nom})) \quad (3\text{-}2)$$

$$\beta = \beta_0 \times \left(\frac{T_j}{T_{nom}}\right)^{TC\beta} \quad (3\text{-}3)$$

Note that the drain-source resistance (R_{ds}) of the MOSFET is the inverse number of drain-source

conductance (G_{ds}).

Next we define a diode function that expresses the voltage-current (V-I) characteristics of the diode device, and express it as Eq. (3-4). It is used to describe the characteristics of two diodes (body diode and breakdown diode) that are depicted in Fig. 3. 2.

$$i_{diode}\left(V_{pn}, V_{on}, R_{on(diode)}, R_{off\,(diode)}\right) := \left[Max\left(Tanh\left(V_{pn}-V_{on}\right), 0.0\right)\times\left(\frac{1.0}{R_{on(diode)}}\right)+\left(\frac{1.0}{R_{off\,(diode)}}\right)\right]\times V_{pn} \tag{3-4}$$

In the following, we derive a system of ordinary differential equations to express the electrical characteristics and self-heating effect of the MOSFET.

As depicted in Fig. 3.1, the drain-source current (I_{ds}) flows along a drain inductance (L_{drain}) and a drain resistance (R_{drain}), and it is described by an ordinary differential equation of Eq. (3-5).

$$V_{dd}-V_{ds}=L_{drain}\frac{dI_{ds}}{dt}+R_{drain}\times I_{ds} \tag{3-5}$$

As depicted in Fig. 3.1 and Fig. 3. 2, the KCL (Kirchhoff's Current Law) with respect to gate node (V_{gs}) is expressed as Eq. (3-6).

$$\frac{V_{gg}-V_{gs}}{R_{gate}}=\left(C_{gd}+C_{gs}\right)\frac{dV_{gs}}{dt}-C_{gd}\frac{dV_{ds}}{dt} \tag{3-6}$$

As depicted in Fig. 3.2, the KCL with respect to drain node (V_{ds}) is expressed as Eq. (3-7). Note that it uses the functions defined by Eqs. (3-3) and (3-4).

$$\begin{aligned}&-C_{gd}\frac{dV_{gs}}{dt}+\left(C_{gd}+C_{ds}\right)\frac{dV_{ds}}{dt}+G_{ds}\left(V_{gs}, V_{th}, \beta, R_{off\,(mos)}\right)\times V_{ds}\\&-i_{diode}\left(-V_{ds}, V_{on(body)}, R_{on(body)}, R_{off\,(body)}\right)\\&+i_{diode}\left(V_{ds}-V_{bv}, V_{on(bkdn)}, R_{on(bkdn)}, R_{off\,(bkdn)}\right)+\frac{V_{ds}}{R_{body}}=I_{ds}\end{aligned} \tag{3-7}$$

The temperature dependence of effective avalanche breakdown voltage ($BV_{ds(eff)}$) is used at our simple electrical power MOSFET model depicted in Fig. 3.2, and it is expressed as Eq. (3-8) [13].

$$BV_{ds(eff)}=BV_{ds}\times\left(1.0+9.5e-4\times\left(T_j-T_{nom}\right)+1.0e-7\times\left(T_j-T_{nom}\right)^2\right) \tag{3-8}$$

As depicted in Fig. 3.1 and Fig. 3. 3, the power dissipation ($G_{\text{mos\_pwr}}$) of the MOSFET flows into the thermal equivalent circuit model, which is a simple linear network that composed of thermal resistances and thermal capacitances. Therefore, it is expressed as Eq. (3-9). Furthermore, by using the device junction-case temperature rise (T_{thi}), the case-ambient temperature (T_{thp}), and ambient temperature (T_{amb}), the device junction temperature (T_j) is calculated by Eq. (3-10).

$$\left.\begin{aligned}&P_{mos}=I_{ds}\times V_{ds}\\&C_{th1}\frac{dT_{th1}}{dt}+\frac{T_{th1}}{R_{th1}}=P_{mos}\\&C_{th2}\frac{dT_{th2}}{dt}+\frac{T_{th2}}{R_{th2}}=P_{mos}\\&C_{th3}\frac{dT_{th3}}{dt}+\frac{T_{th3}}{R_{th3}}=P_{mos}\\&C_{th4}\frac{dT_{th4}}{dt}+\frac{T_{th4}}{R_{th4}}=P_{mos}\\&C_{th5}\frac{dT_{th5}}{dt}+\frac{T_{th5}}{R_{th5}}=P_{mos}\\&C_{th6}\frac{dT_{th6}}{dt}+\frac{T_{th6}}{R_{th6}}=P_{mos}\\&C_{thp}\frac{dT_{thp}}{dt}+\frac{T_{thp}}{R_{thp}}=P_{mos}\end{aligned}\right\} \tag{3-9}$$

$$T_j=T_{th1}+T_{th2}+T_{th3}+T_{th4}+T_{th5}+T_{th6}+T_{thp}+T_{amb} \tag{3-10}$$

In Section IV, we verify our equation-based modeling and electro-thermal coupling circuit analysis with respect to the UIS test circuit.

4 Experimental Results

As described above, we derived the system of ordinary differential equations. We develop a notebook source code and implement it into Mathematica. (See the source code of Appendix A.) We define two node voltages (V_{gs}, V_{ds}), drain-source current (I_{ds}), six device junction-case temperature rises (T_{th1}, T_{th2}, T_{th3}, T_{th4}, T_{th5}, T_{th6}), and case-ambient temperature rise (T_{thp}) as unsolved variables. The initial values at time domain t=0 of these unsolved variables are set in the following: V_{gs}=0.0 [V], V_{ds}=0.0 [V], I_{ds}=0.0 [A], T_{th1}=0.0 [K], T_{th2}=0.0 [K], T_{th3}=0.0 [K], T_{th4}=0.0 [K], T_{th5}=0.0 [k], T_{th6}=0.0 [K].

Furthermore, the value of each parameter in the system of ordinary differential equations is set the same as that of our previous work presented with [13]. Note that the parameter values are based on

the datasheet and application notes [5], [9]-[10] released by Fairchild Semiconductor. (See [13] for more details.) We show the values of main model parameters and temperature coefficients at room temperature in the following: L_{drain}=0.1e-3 [H], R_{drain}=0.3 [Ohm], V_{dd}=41.0 [V], C_{ds}=2.65e-9 [F], C_{gs}=4.40e-9 [F], C_{gd}=1.70e-9 [F], R_{gate}=50.0 [Ohm], T_{nom}=298.15 [K], V_{th0}=2.8 [V], $R_{off(mos)}$=1.0e12 [Ohm], R_{mos_body}=1.0e15 [Ohm], V_{th0}=2.8 [V], β_0=40.0 [A/V2], BV_{dss}=69.3 [V], TCV_{th}=-3.57 [1/K], and $TC\beta$=-2.1 [-], $R_{on(body)}$=0.118 [Ohm], $R_{off(body)}$ =1.0e12 [Ohm], $R_{on(bkdn)}$=0.118 [Ohm], $R_{off(bkdny)}$ =1.0e12 [Ohm], V_{on}=0.6 [V], V_{br}=BV_{dss}, C_{th1}=6.45e-3 [J/K], C_{th2}=3.00e-2 [J/K], C_{th3}=1.40e-2 [J/K], C_{th4}=1.65e-2 [J/K], C_{th5}=4.85e-2 [J/K], C_{th6}=1.00e-1 [J/K], C_{thp}=1.00e-2 [J/K], R_{th1}=3.24e-3 [K/W], R_{th2}=8.08e-3 [K/W], R_{th3}=2.28e-2 [K/W], R_{th4}=1.00e-1 [K/W], R_{th5}=1.10e-1 [K/W], R_{th6}=1.40e-1 [K/W], R_{thp}=62.0 [K/W], T_{amb}= T_{nom}.

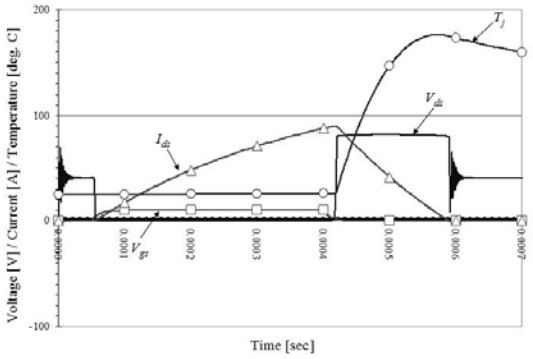
As our experimental verification, we ran the circuit analysis with Mathematica on HP dv9700 (OS Windows 7, CPU Intel(R) Core(TM) 2.5GHz, RAM 8.00 GB). And we obtained the solutions for the unsolved variables by numerical module NDsolve( ), and its run time (CPU time) is 91.2 [sec]. Figure 5.1 (1) depict the circuit analysis results in the time domain. The value of the device junction temperature (T_j) is calculated with the values of size device junction-case temperature rises (T_{th1}, T_{th2}, T_{th3}, T_{th4}, T_{th5}, T_{th6}) and case-ambient temperature rises (T_{thp}, T_{amb}) by Eq. (3-10). Note that the device junction temperature (T_j) is expressed by unit of deg. C in the Fig. 5.1.

As other reference, we used an accurate PSPICE electro-thermal power MOSFET model [5], [9]-[10] released by Fairchild Semiconductor, and simulated the same UIS test circuit depicted in Fig. 3.1, with a powerful circuit simulator called TINA-TI (Texas Instruments version of PSPICE) [17] from Texas Instruments. In this case, the run time with the same computer mentioned above is 26.5 [sec]. Figure 5.1 (2) depict the circuit simulation results obtained by TINA-TI.

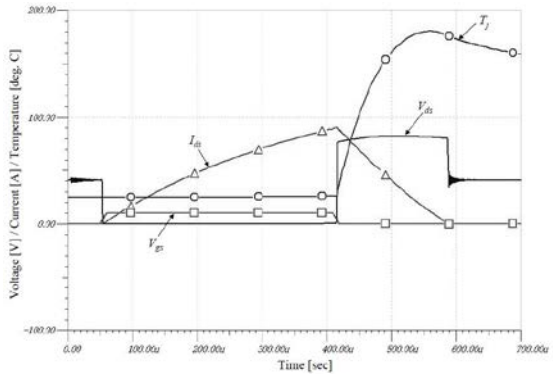
Furthermore, we used a very simple XSPICE electro-thermal power MOSFET model [13] released by our previous work, and simulated the same UIS test circuit depicted in Fig. 3.1, with a free circuit simulator called NGSPICE/XSPICE from the gEDA Project [14] and the Georgia Institute of Technology. [20]. In this case, the run time with the same computer mentioned above is 6.1 [sec]. Figure 5.1 (3) depict the circuit simulation results obtained by NGSPICE/XSPICE.

As depicted in Fig. 5.1 (1), the circuit analysis results on our equation-based modeling with Mathematica have some oscillations. But they are almost consistent with those of other two reference cases, and hence demonstrate the adequacy of our technique for electro-thermal modeling and circuit analysis.

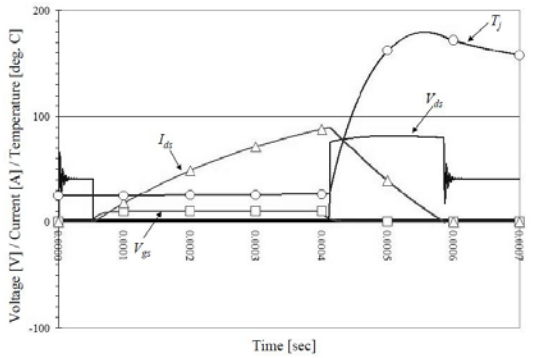
However, its run time increases more than those of other two cases. The reason is due to the performance of the numerical solver (NDsolve( )) of Mathematica.



(1) Mathematica with our equation-based model



(2) TINA-TI (PSPICE) with accurate model of [5], [9]-[10]



(3) NGSPICE/XSPICE with our simple model of [13]

Fig. 5.1: Simulation results of UIS test circuit.

5 Conclusions

We have proposed a new technique for the electro-thermal modeling and reliability circuit analysis with Mathematica. It starts with the modeling of a power MOSFET circuit as a system of ordinary differential equations, and uses a numerical solver of Mathemtica to obtain a solution of the system.

Furthermore, we applied our technique to electro-thermal and reliability circuit analysis of an UIS test circuit. Our technique was demonstrated by experimental results. They also revealed that the numerical solver of Mathematica is capable of circuit analysis such as that of SPICE (a circuit simulator)..

However the solver is more than 10 times slower than that of SPICE. We are improving the solver of Mahematica in order to reduce the run time.

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Appendix A: Our notebook source codes with Mathematica

```
(*** diode function ***)
id[Vpn_,Von_,Rondiode_,Roffdiode_]=(Max[Tanh[Vpn-Von],0.0]*(1.0/Rondiode)+(1.0/Roffdiode))*Vpn;
(*** mos drain-source conductance function ***)
Gds[Vgs_,Vth_,β_,Roffmos_,Tjuncnom_,Tjunc_,TCB_,TCV_]=(Max[Tanh[Vgs-Vth*(1.0+TCV*(Tjunc-Tjuncnom))],0.0]*β*(
Tjunc/Tjuncnom)^TCB*(Vgs-Vth*(1.0+TCV*(Tjunc-Tjuncnom)))+(1.0/Roffmos));
(*** gate input pulse function ***)
fpulse[x_Real,delay_,rise_,width_,fall_,periode_,lowval_,highval_]=Which[x<=delay,lowval,
Mod[x-delay,periode]>rise+width+fall,lowval,
Mod[x-delay,periode]>rise+width,(lowval-highval)/fall*(Mod[x-delay,periode]-rise-width)+highval,
Mod[x-delay,periode]>rise,highval,
Mod[x-delay,periode]>0.0,(highval-lowval)/rise*(Mod[x-delay,periode])+lowval,
Mod[x-delay,periode]<=0.0,lowval];
(*** device junction temperature ***)
Tj[DTp_,DT6_,DT5_,DT4_,DT3_,DT2_,DT1_]=DTp+DT6+DT5+DT4+DT3+DT2+DT1+298.15;
(*** unsolved variables ***)
Clear[i, vg, vd,Tp,T6,T5,T4,T3,T2,T1];
(*** a system of ordinary differential equations for an electronic circuit ***)
eqns={Ldrain*(i^')[t]==Vdd-vd[t]-Rdrain*i[t],
(Cgd+Cgs)*vg'[t]-Cgd*vd'[t]==(fpulse[t,Delay,Rise,Width,Fall,Periode,Lowval,Highval]-vg[t])/Rgate,
-Cgd*vg'[t]+(Cgd+Cds)*vd'[t]==0.0-Gds[vg[t],Vth,β,Roffmos,Tnom,Tj[Tp[t],T6[t],T5[t],T4[t],T3[t],T2[t],T1[t]],TCB,TCV]*vd
[t]+id[0.0-vd[t],Von,Rondiode,Roffdiode]-id[vd[t]-(Vbv*(1.0+9.5*10^-4*(Tj[Tp[t],T6[t],T5[t],T4[t],T3[t],T2[t],T1[t]]-Tnom)+1
.0*10^-7*(Tj[Tp[t],T6[t],T5[t],T4[t],T3[t],T2[t],T1[t]]-Tnom)^2)),Von,Rondiode,Roffdiode]-vd[t]/Rbody+i[t],
(*** a system of ordinary differential equations for a thermal circuit ***)
Cthp*Tp'[t]==i[t]*vd[t]-Tp[t]/Rthp,
Cth6*T6'[t]==i[t]*vd[t]-T6[t]/Rth6,
Cth5*T5'[t]==i[t]*vd[t]-T5[t]/Rth5,
Cth4*T4'[t]==i[t]*vd[t]-T4[t]/Rth4,
Cth3*T3'[t]==i[t]*vd[t]-T3[t]/Rth3,
Cth2*T2'[t]==i[t]*vd[t]-T2[t]/Rth2,
Cth1*T1'[t]==i[t]*vd[t]-T1[t]/Rth1,
(*** initialization ***)
i[0]==0.0, vd[0]==0.0, vg[0]==0.0, Tp[0]==0.0, T6[0]==0.0, T5[0]==0.0, T4[0]==0.0, T3[0]==0.0, T2[0]==0.0, T1[0]==0.0
};
(*** input parameters ***)
eqns                                                                                                    =
eqns/.{Ldrain->1.0*10^-4,Rdrain->0.3,Vdd->41.0,Cgd->1.7*10^-9,Cgs->4.4*10^-9,Cds->2.65*10^-9,Rgate->50.0,Delay->0.05
*10^-3,Rise->0.01*10^-3,Width->0.35*10^-3,Fall->0.01*10^-3,Periode->1.0*10^-3,Tnom->298.15,
Lowval->0.0,Highval->10.0,Vth->2.8,β->40.0,Roffmos->1.0*10^12,Von->0.6,Vbv->69.3,Rondiode->0.118,Roffdiode->1.0*10
^12,Rbody->1.0*10^15,Cthp->1.0*10^-2,Rthp->62.0,Cth6->1.0*10^-1,Rth6->1.4*10^-1,Cth5->4.85*10^-2,Rth5->1.1*10^-1,Ct
h4->1.65*10^-2,Rth4->1.0*10^-1,Cth3->1.40*10^-2,Rth3->2.28*10^-2,Cth2->3.00*10^-2,Rth2->8.08*10^-3,Cth1->645*10^-3
,Rth1->3.24*10^-3,TCB->-2.1,TCV->-3.57*10^-3} ;
(*** call NDSolve() ***)
sol[v_]:= NDSolve[(eqns)/. Vdd->v,{i,vg, vd,Tp,T6,T5,T4,T3,T2,T1},{t,0,2.0*10^-3},MaxStepSize->0.1,MaxSteps->1000000];
(*** plots ***)
Do[Print[Plot[Evaluate[vd[t]/. sol[Vdd]],{t,0,2.0*10^-3},PlotLabel->Vdd]],{Vdd,41.0,41.0,41.0}];
Do[Print[Plot[Evaluate[i[t]/. sol[Vdd]],{t,0,2.0*10^-3},PlotLabel->Vdd]],{Vdd,41.0,41.0,41.0}];
Do[Print[Plot[Evaluate[Tj[Tp[t],T6[t],T5[t],T4[t],T3[t],T2[t],T1[t]]-273.15/.
sol[Vdd]],{t,0,2.0*10^-3},PlotLabel->Vdd]],{Vdd,41.0,41.0,41.0}];
```